REMARKS

The Examiner's Office Action of May 5, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

By the above actions, claims 1, 3 and 7 have been amended. Accordingly, claims 1-10 are pending for consideration, of which claim 1 is independent. In view of these actions and the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1-10 stand rejected under 35 U.S.C. §103(a) as unpatentable over Applicants' Admitted Prior Art in view of Hideki (JP patent No. 11040801). This sole rejection is respectfully traversed at least for the reasons provided below.

In response to the rejection, Applicants have amended claim 1, as shown above, to further clarify and distinguish the presently claimed invention over the cited prior art. Support for the amendment to claim 1 is found in Fig. 2D and the description thereof in the present specification.

In order to explain and compare the invention of claim 1 and that of the cited prior art, Applicants will refer now to, e.g., Fig. 2A-2D of the present invention with numerical labels for the features recited therein. As illustrated in Figs. 2A-2D, the method for manufacturing a semiconductor device recited in claim 1 comprises:

a) a first step of forming a gate electrode 13 on a semiconductor region 11 via a gate insulative film 12;

b) a second step of forming an amorphous layer 19A in an upper portion of the semiconductor region 11 by implanting ion of a group IV element into the semiconductor region 11 using the gate electrode 13 as a mask;

c) after the second step, a third step of implanting a first impurity of a first conductivity type into the semiconductor region 11 in which the amorphous layer 19A is formed using the gate electrode 13 as a mask with an implantation projected range such that the first impurity reaches a position deeper than the amorphous layer 19A; and

d) after the third step, a fourth step of subjecting the upper portion of the semiconductor region 11 to thermal annealing so as to form a dislocation loop defect layer 19 and an extension high concentration diffusion layer 16 of the first conductivity type through

diffusion of the first impurity, the extension high concentration diffusion layer having a junction at a position deeper than the dislocation loop defect layer 19.

In other words, according to amended claim 1, the first impurity is implanted into the semiconductor region in which the amorphous layer is formed, and then the thermal annealing is performed so as to form the dislocation loop defect layer and the extension high concentration diffusion layer.

In comparison with the claimed invention, the Admitted Prior Art, as illustrated in Figs. 13A-13C of the present application, relates to a method for manufacturing a semiconductor device which comprises:

a) a step of forming a gate electrode 104 on a semiconductor region 101 via a gate insulating film 103;

b) a step of forming a second ion implantation layer 106A by implanting a p-type impurity ion in the semiconductor region 101 using the gate electrode 104 as a mask; and

c) a step of performing thermal annealing so as to form a p-type extension high concentration diffusion layer 106 including the second ion implantation layer 106A.

Applicants respectfully submit that the differences between the invention recited in claim 1 and the admitted prior art are as follows:

1) The Admitted Prior Art fails to disclose the second step of forming an amorphous layer in the upper portion of the semiconductor region by implanting ion of a group IV element into the semiconductor region.

2) In the Admitted Prior Art, there is no step of forming the amorphous layer, hence no amorphous layer is formed in the semiconductor substrate 101 when forming the second ion implantation layer 106A by implanting the p-type impurity ion. On the other hand, in the third step of the presently claimed invention, the first impurity of a first conductivity type is implanted into the semiconductor region in which the amorphous layer is formed. Thus, the state of the underlying substrate of the present invention is different from that of the Admitted Prior Art.

3) The Admitted Prior Art fails to disclose that a dislocation loop defect layer is formed when forming the p-type extension high concentration diffusion layer 106 comprising the second ion implantation layer 106A by the thermal annealing.

With respect to Hideki, as illustrated in Figs. 1(a)-1(c) and Fig. 2(a)-2(c), a method for manufacturing a semiconductor device is disclosed. The method of Hideki includes:

a) a first step of forming a gate electrode 9 on a substrate 3 via a gate insulating film 7;

b) a second step of forming an amorphous layer 13 in the substrate 3 by performing an ion implantation 11 into the substrate 3 using the gate electrode 9 as a mask;

c) after the second step, a third step of subjecting the substrate 3 to a first thermal annealing so as to form a dislocation loop 15 within the substrate 3;

d) after the third step, a fourth step of forming a sidewall insulating films 19 including a diffusion source insulating film 17 containing dopant on each side of the gate electrode 9; and

e) after the fourth step, a fifth step of subjecting the substrate 3 to a second thermal annealing to diffuse impurities into the substrate 3 in solid phase from the sidewall insulating films 19, so as to form an LDD diffusion layer 21.

Applicants respectfully submit that the differences between the invention recited in claim 1 and the invention disclosed in Hideki are as follows:

1) In Hideki, after forming the amorphous layer in the substrate, the first thermal annealing is carried out so as to form the dislocation loop, and then the LDD diffusion layer is formed by diffusing impurities into the substrate in solid phase. In other words, in Hideki, the first thermal annealing for forming the dislocation loop and the second thermal annealing for forming the LDD diffusion layer are independently carried out. On the other hand, in the present invention of amended claim 1, the upper portion of the semiconductor region is subjected to the thermal annealing so as to form the dislocation loop defect layer and an extension high concentration diffusion layer of the first conductivity type.

2) Hideki fails to teach, disclose or suggest the third and fourth steps of the amended claim 1. Specifically, Hideki does not teach, disclose or suggest the third step of implanting a first impurity of a first conductivity type into the semiconductor region in which the amorphous layer is formed using the gate electrode as a mask with an implantation projected range such that the first impurity reaches a position deeper than the amorphous layer, and the fourth step of subjecting the upper portion of the semiconductor region to thermal annealing so as to form a dislocation loop defect layer, and an extension high

concentration diffusion layer of the first conductivity type through diffusion of the first impurity, the extension high concentration diffusion layer having a junction at a position deeper than the dislocation loop defect layer.

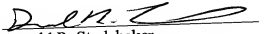
The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As APA and Hideki are deficient as set forth above, their combination in the §103(a) rejection of amended claim 1 and its dependent claims 2-10 is improper.

Claims 3 and 7 have been amended to correct minor typographical errors.

In view of the amendments and arguments set forth above, Applicants respectfully request reconsideration and withdrawal of the pending §103(a) rejection.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,



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